Reducing MLC Flash Memory Retention Errors through Programming Initial Step Only

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Introduction
The floating-gate of a memory cell stores a number of electrons, which affects the cell’s threshold voltage, \( V_{th} \). The value of \( V_{th} \) is measured to determine the state of a cell. A retention error is caused by electron leakage and de-trapping phenomenon over time, which shift the \( V_{th} \) of a programmed cell to a lower level across its left reference voltage. Retention error has been identified as the dominant flash memory error. To compensate a cell’s charge loss over time, and thus, correct its retention error, an intuitive solution is to inject an appropriate amount of electrons into a cell so that its \( V_{th} \) can be pushed back to its original level.

An Analytical Model

- **Threshold voltage distribution**
  \[
  f(x) = \sum_{j=1}^{3} \frac{1}{4\sqrt{2\pi}\sigma_j} \exp\left(-\frac{(x-\mu_j)^2}{2\sigma_j^2}\right)
  \]

- **Voltage shift due to retention and a PISO operation**
  \[
  f(x) = \sum_{j=1}^{3} \frac{1}{4\sqrt{2\pi}\sigma_j} \exp\left(-\frac{(x-n\Delta V_{th})^2}{2\sigma_j^2}\right)
  \]

- **Voltage shift due to retention**
  \[
  1 - \alpha(1)\mu_j^2
  \]

- **The number of PISO operations applied can be solved by the error minimization problem**
  
  \[
  \min \left\{ \frac{1}{4}Q_0\left(\Delta V_{th}\right) + \frac{1}{4}Q_0\left(\Delta V_{th}\right) + \frac{1}{4}Q_0\left(\Delta V_{th}\right) + \frac{1}{4}Q_0\left(\Delta V_{th}\right) \right\}
  \]

Testing Methodology

- **Variable Relaxation Aging**
  - Flash memory are supposed to be used in a 3 years @ 45 C environment.
  - Baking: 70.6 hours @100C

- **Retention acceleration**
  - Programmed flash memory devices are stored under 40C for 3 months.
  - Baking: 63 hours @ 70C.

Evaluation Results

- **Effectiveness**
  - The number of bit errors rapidly decreases within 10 PISOs.
  - Further increasing the number of PISOs enlarges bit errors.

- **Comparisons with read disturb**
  - The read disturb scheme demands a much larger number of operations in order to reduce a similar number of errors.
  - An appropriate number of PISO operations

Conclusions

PISO is efficient and effective compared to other types of retention error reduction methods. It can be readily implemented in either the FTL of an SSD or in a flash file system. It is simple and do not require a prior knowledge of the original stored data.

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References


1. Computational Science Research Center, SDSU
2. Computer Science Department, SDSU
3. Seagate Technology.