Reducing MLC Flash Memory Retention Errors through Programming Initial Step Only

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Introduction

The floating-gate of a memory cell stores a number of electrons, which affects the cell's threshold voltage, V_{th}. The value of V_{th} is measured to determine the state of a cell. A retention error is caused by electron leakage and de-trapping phenomenon over time, which shift the $\mathbf{V}_{th}$ of a programmed cell to a lower level across its left reference voltage. Retention error has been identified as the dominant flash memory error. To compensate a cell's charge loss over time, and thus, correct its retention error, an intuitive solution is to inject an appropriate amount of electrons into a cell so that its $\mathbf{V}_{th}$ can be pushed back to its original level.

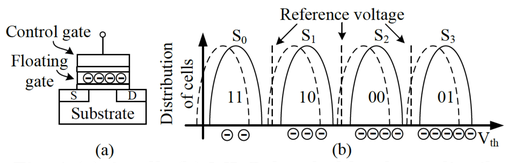


Fig. 1 (a) A cell; (b) MLC threshold voltage distribution.

The PISO Approach

- PISO exploits the first programming-and-verifying step in a programming operation by programming the data corresponding to the safe V_{th}.

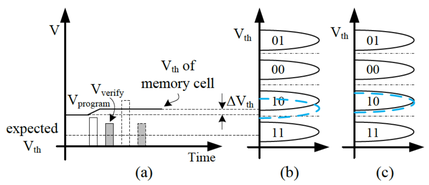


Fig. 2 (a) A PISO operation; (b) before; (c) after PISO.

- The safe threshold voltage
  - ★ LSB page: data '1'
  - ★ MSB page: the data stored in its associated LSB page.

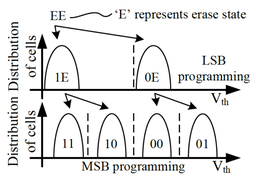
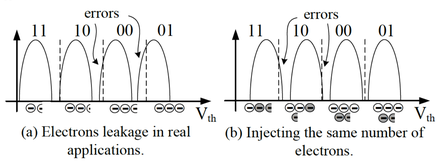


Fig. 3 Programming an MLC cell.

- ★ MSB PISO cost is larger than LSB PISO cost.
- Preventing the excessive use of PISO



An Analytical Model

- Threshold voltage distribution

$$f(x) = \sum_{s=0}^{3} \frac{1}{4\sqrt{2\pi}\delta_s} exp\{\frac{-(x-\mu_s)^2}{2\delta_s^2}\}$$

- Voltage shift due to retention and a PISO operation

Voltage shift after *m* PISO operations

$$f(x) = \sum_{s=0}^{3} \frac{1}{4\sqrt{2\pi}\delta_s} exp\{\frac{-[x + m\Delta V_{th,S}^{R} - (1-\alpha(t))\mu_s]^2}{2\delta_s^2}\}$$

Voltage shift due to retention

- The number of PISO operations applied can be solved by the error minimization problem

$$min[\frac{1}{4}Q_{S_0}(\frac{|\Delta_0|}{\delta_0}) + \frac{1}{4}Q_{S_1}(\frac{|\Delta_1|}{\delta_1}) + \frac{1}{4}Q_{S_1}(\frac{|\Delta_2|}{\delta_1}) + \frac{1}{4}Q_{S_2}(\frac{|\Delta_3|}{\delta_2}) + \frac{1}{4}Q_{S_2}(\frac{|\Delta_4|}{\delta_2}) + \frac{1}{4}Q_{S_3}(\frac{|\Delta_5|}{\delta_3})],$$

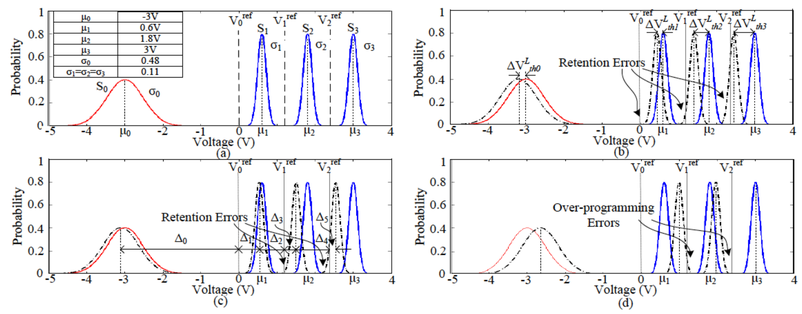


Fig. 5 V_{th} distributions; (a) normal; (b) left shifted; (c) with inadequate number of PISOs; (d) over-programmed.

Testing Methodology

- Variable Relaxation Aging
  - ❖ Flash memory are supposed to be used in a 3 years @ 45 C environment.
  - ❖ Baking: 70.6 hours @100C

Group	P/Es
A	1 K
B	2 K
C	4 K
D	6 K
E	12 K
F	20 K

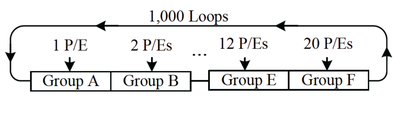


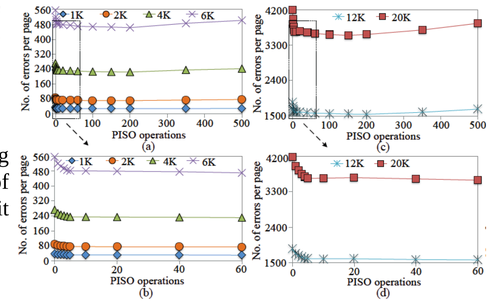
Fig. 6 Variable relaxation cycling procedure.

- Retention acceleration
  - ❖ Programmed flash memory devices are stored under 40C for 3 months.
  - ❖ Baking: 63 hours @ 70C.

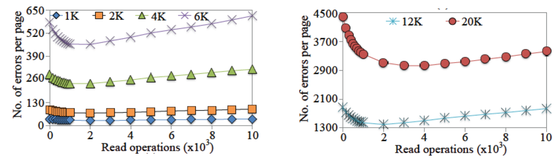
	Flash A	Flash B
Page size	16 KB	16 KB
Pages per block	512	256
Blocks per plane	2,048	2,048
Plane per die	2	1
Dies per package	4	2
Read latency (μs)	47	47
LSB page write latency (μs)	471	566
MSB page write latency (μs)	1,353	1,870

Evaluation Results

- Effectiveness
  - ★ The number of bit errors rapidly decreases within 10 PISOs.
  - ★ Further increasing the number of PISOs enlarges bit errors.

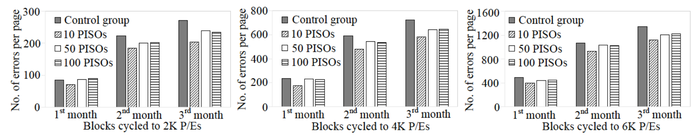


- Comparisons with read disturb



❖ The read disturb scheme demands a much larger number of operations in order to reduce a similar number of errors.

- An appropriate number of PISO operations



- ★ Applying PISO operations 10 times each month can reduce the largest number of retention errors among the four groups.
- ★ A dynamic retention error detection mechanism that periodically samples retention errors can be applied.

Conclusions

PISO is efficient and effective compared to other types of retention error reduction methods. It can be readily implemented in either the FTL of an SSD or in a flash file system. It is simple and do not require a prior knowledge of the original stored data.

Acknowledgement

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References

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